REMARKS

Claims 1, and 3-12 are pending in the application. Claims 1 and 7-10 were rejected under 35 U.S.C. § 102(e). Claims 2-6 and 11 were rejected under 35 U.S.C. § 103(a).

Rejection Under 35 U.S.C. § 102(e)

Claims 1 and 7-10 were rejected as being anticipated under 35 U.S.C. §102(e) by U. S. Patent Number 6,812,145 issued to Ma on November 2, 2004.

Applicants have avoided this ground of rejection for the following reasons.

First, applicants have amended independent claim 1 to include therein the limitations from claim 2. As a result, Ma does **not** teach applicants' independent claim 1 limitation, as amended, that now recites:

> "wherein upon exposure of the conduction layer during an etch of the wafer portion, the conduction layer serves to dissipate a portion of a charge buildup on the wafer portion, and wherein the conduction layer is electrically coupled with a silicon layer of the wafer portion; and wherein removal of a portion of the silicon layer from the wafer portion during the etch serves to expose the conduction layer."

Instead, Ma teaches a processing step that deposits a protective layer of conductive material over the top of the dielectric hardmask layer, including on the floor and sidewalls of the contact opening, as stated in column 5, lines 62-65. By contrast, applicants' claimed invention exposes, rather than deposits, a conduction layer in the wafer. As known by those skilled in the art, exposure means making something visible. To deposit means to put something down or in place. Thus, Ma is missing the element, "upon exposure of the conduction layer during an etch of the wafer portion, the conduction layer serves to dissipate a portion of a charge buildup on the wafer portion", as recited in applicants' claim 1.

Second, Ma does **not** disclose "removal of a portion of the silicon layer from the wafer portion during the etch serves to expose the conduction layer", as recited in applicants' claim 1. Instead, Ma discloses that when the protective

conductive layer is in place, a layer of photoresist is applied, and covers the protective conductive layer. The photoresist layer is patterned, by being exposed and developed, leaving a portion of the protective conductive layer, overlying a second dielectric hardmask, covered by photoresist, and a portion exposed, as stated in column 6, lines 21-29. By contrast, removal of a portion of the silicon layer from the wafer portion during the etch serves to expose the conduction layer, as recited in applicants' claim 1.

Third, Ma does not disclose "wherein the conduction layer is electrically coupled with a silicon layer of the wafer portion", as recited in applicants' claim 1. Instead, Ma discloses that an electrical contact opening runs from the upper surface of the dielectric hardmask layer, downward through the hardmask layer and underlying dielectric layer, terminating at the upper surface of underlying etch stop layer, as stated in column 5, lines 56-60. Thus, Ma is missing the conduction layer is electrically coupled with a silicon layer of the wafer portion element, as recited in applicants' claim 1.

Thus, the clear teaching of Ma is that the conduction layer is **not** exposed during an etch of the wafer portion, and the conduction layer is **not** electrically coupled with a silicon layer of the wafer portion, and a portion of the silicon layer is **not** removed from the wafer portion during the etch to serve to expose the conduction layer.

In view of the foregoing, applicants submit that Ma does not describe each and every element of claim 1, and therefore claim 1 is not anticipated by Ma. Since claims 7-10 depend from allowable claim 1, these claims are also allowable over Ma.

Rejection Under 35 U.S.C. § 103(a)

Claims 2-6 and 11 were rejected under 35 U.S.C. §103(a) as being unpatentable over Ma in view of U. S. Patent Number 5,865,938 issued to Peeters et al. on February 2, 1999.

Applicants have avoided this ground of rejection for the following reasons.

First, applicants have canceled claim 2. Claims 3-6 and 11 depend from independent claim 1. Ma does **not** teach or suggest claim 1, as shown hereinabove. The Office Action has cited Peeters only for its teaching that electrical biases are at the lower part of a conductive semiconductor layer. Thus, the Office Action seems to indicate, and applicants agree, that Peeters does **not** supply the elements of applicants' claim 1 that were shown hereinabove not to be taught by Ma.

Therefore the combination of Ma with Peeters does not teach or suggest all of the limitations in applicants' claim 1, and therefore claim 1 is allowable over the proposed combination.

Since claims 3-6 and 11 depend from claim 1, these dependent claims are also allowable over the proposed combination.

Second, applicants' claim 11 recites, "wherein the conduction layer comprises a thickness in the range of about one half micrometer ("μm") to about two micrometers."

As stated in the Office Action, Ma does **not** teach the specific thickness of his conductive layer. Applicants respectfully object to the Examiner rejecting applicants' claim 11 without a reference document being cited as the basis for the rejection.

New Claim

New claim 12 has been added. Claim 12 includes a limitation directed to the type of etch process and is submitted to be patentable because a Deep Reactive Ion Etch (DRIE) and a Bosch process are not taught by the cited references. No new matter has been added.

Conclusion

It is respectfully submitted that the Office Action's rejections have been overcome and that this application is now in condition for allowance. Reconsideration and allowance are, therefore, respectfully solicited.

If, however, the Examiner still believes that there are unresolved issues, he is invited to call applicants' attorney so that arrangements may be made to discuss and resolve any such issues.

Respectfully submitted,

By _____

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